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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/901,746	07/10/2001	Yoshinori Takahashi	36856.526	8463

7590 07/09/2002  
KEATING & BENNETT LLP  
Suite 312  
10400 Eaton Place  
Fairfax, VA 22030

EXAMINER

NGUYEN, HIEP

ART UNIT	PAPER NUMBER
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2816

DATE MAILED: 07/09/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/901,746

Applicant(s)

TAKAHASHI, YOSHINORI

Examiner

Hiep Nguyen

Art Unit

2816

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 10 July 2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-21 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-21 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413) Paper No(s) \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

## DETAILED ACTION

### *Claim Rejections - 35 USC § 112*

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 2 and 16 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Correction and /or clarification is required.

Regarding claims 2 and 16, the recitation "said portion of said one of the at least two conductor layers that is omitted is disposed inside said multi-layer substrate" is indefinite because it is not clear how a portion of a conductor can be disposed inside a substrate.

### **Claim Rejections - 35 USC § 102**

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Mandai et al. (US Pat. 5,227,739).

Regarding claim 1, figure 4 of Mandai shows a resonator comprising: a multi-layer substrate having an upper and lower surface, and including at least two conductor layers (3,5,7) which include at least two grounding conductor layers (3,5,7) and a plurality of dielectric layers (2a-2g), one of the at least two grounding conductor layers (3) being disposed on the lower surface of the multi-layer substrate; a strip line (4) disposed between the at least two grounding conductor layers (3,5); a microstrip line (9) disposed on the upper surface of said multi-layer substrate; and a through hole (V1) formed in said dielectric layers to connect said strip line to said microstrip line; wherein at least a portion of the one of the at least two conductor layers that is closest to said microstrip line and faces the microstrip line is omitted ( V1 of conductor 7).

Regarding claims 2, 3, 4 and 5 the portion of said one of the at least two conductor layers that is omitted (7) is disposed "inside" said multi-layer substrate and is arranged such that said grounding conductor layer disposed on the lower surface of said multilayer substrate faces said microstrip line (9). The omitted portion defines the opening in the one of the least two conductor layers and the shape of the hole is rectangular. The strip line (4) has an U-shaped configuration.

Regarding claims 6 and 7, the strip line is (4) and the micro strip line is (9).

Regarding claim 8, 9, 10, 11, 12 and 13, figure 4 of Mandai shows a resonator comprising: a multi-layer substrate having an upper and lower surface, and including at least two conductor layers (3, 5, 7) which include at least two grounding conductor layers (3,5,7) and a plurality of dielectric layers (2a-2g), one of the at least two grounding conductor layers (3,5) being disposed on the lower surface of the multi-layer substrate, and one of the at least two conductor layers (5,7) that is closest to said microstrip line and faces the microstrip line has an opening (V1) formed therein; a strip line (4) disposed between the at least two grounding conductor layers (3,5); a microstrip line (9) disposed on the upper surface of said multi-layer substrate; and a through hole (V1) formed in said dielectric layers to connect said strip line to said microstrip line. The grounding conductor layer (3) faces the strip line (4). the opening (V1) has a rectangular shape and the strip line (4) has an U- shaped configuration. The resonator comprises only one strip line (4).

Regarding claims 14 and 15, figure 4 of Mandai shows a voltage controlled oscillator comprising: a resonator including: a multi-layer substrate having an upper and lower surface, and including at least two conductor layers (3,5,7) which include at least two grounding conductor layers and a plurality of dielectric layers (2a-2g), one of the at least two grounding conductor layers being disposed on the lower surface of the multi-layer substrate; a strip line (4) disposed between the at least two grounding conductor layers; a microstrip line (9) disposed on the upper surface of said multi-layer substrate; and a through hole (V1) formed in said dielectric layers to connect said strip line to said microstrip line; wherein at least a portion of the one of the at least two conductor layers (7) that is closest to said microstrip line (9) and faces the microstrip line is omitted; and a plurality of electronic component elements disposed on the upper surface (2g) of

the multi-layer substrate and arranged to define a circuit and inherently the plurality of the electronic component elements and the resonator are electrically connected to each other.

Regarding claim 16, said portion of said one of the at least two conductor layers (5,7) that is omitted is disposed "inside" said multi-layer substrate and is arranged such that said grounding conductor layer (3) disposed on the lower surface of said multi-layer substrate faces said microstrip line (9).

Regarding claims 17, 18, 19, 20 and 21, the portion of said one of the at least two conductor layers (5,7) that is omitted defines an opening in said one of the at least two conductor layers and the opening has a rectangular shape. The strip line (4) has a U shape. The VCO has only one strip line (4) and one microstrip line (9).

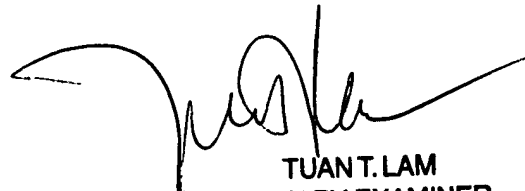
### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner Hiep Nguyen whose telephone number is (703) 305-0127. The examiner can normally be reached on Monday to Friday from 7:30 A.M. to 4:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached on (703) 308-4876. The fax phone number for this Group is (703) 308-6251.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.

Hiep Nguyen  
Examiner  
07-03-02



TUAN T. LAM  
PRIMARY EXAMINER